CHIPS.
Monthly Newsletter
June 2010

Put first things first.

(Stephen R. Covey)

"De quoi s'agit-il?"

The statement from Stephen Covey sounds simple: just do the things that come first. However, what comes first? In my personal opinion, the separation of the problem into four quadrants as proposed by Covey does not really help. The crucial element is the problem analysis. If one does not understand what is going on, a decision into which quadrant a problem has to be sorted, is not possible. The key phrase here is 'problem analysis'. It is unbelievable how many people start with a solution to a problem before they have really understood the problem itself. Over the past couple of months, I have seen numerous such bad examples. A customer tells me that the product has this or that failure/problem but unfortunately, he does not take into account that the environment in which he is using our product, lies outside the specs range. Our engineers try to find the root cause of the problem but cannot find anything. A huge yet worthless effort spent trying to make the customer happy. A totally useless undertaking: a lot of frustration, unhappy customers, and a lot of time and energy poured down the drain.

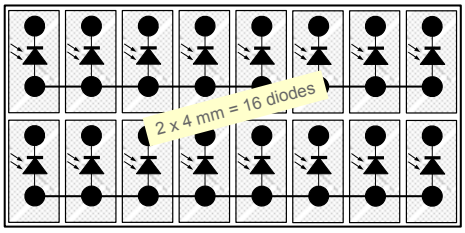
What is my point? It is simple: Most of the time people are careless about how they interact with others. They do not first ask themselves "De quoi s'agit-il?" as the French do, or in good English "What's the matter?". They say "This is the problem" and "You have to solve it". They do not provide the whole picture and (unintentionally) leave others fumbling in the dark. Mistake number one! However, the party who is supposed to solve the problem says to himself: "He is my customer; customers command, we obey and so I have to solve his problem". Good guy, but running in the wrong direction. Mistake number two! Why? Because he should immediately become an interviewer and ask the customer question after question in order to understand the whole situation. Try it and you will be astonished how little you knew about the real situation at the beginning. And, after getting a more complete picture, you will be astonished again when you find out how simple the solution can be. But please don't get me wrong. A complete picture is put together, not by adding thousands of details (as people very often think) but by simply extracting the relevant aspects only. Quality before quantity!

To live a more balanced existence, you have to recognize that being efficient does not mean doing everything at once, the very moment it comes along. There is no need to overextend yourself. All it takes is realizing that it is all right to say "Wait a minute" and then focus on trying to understand the problem. You are then in a position where you can only win. Guaranteed!

Beat De Coi

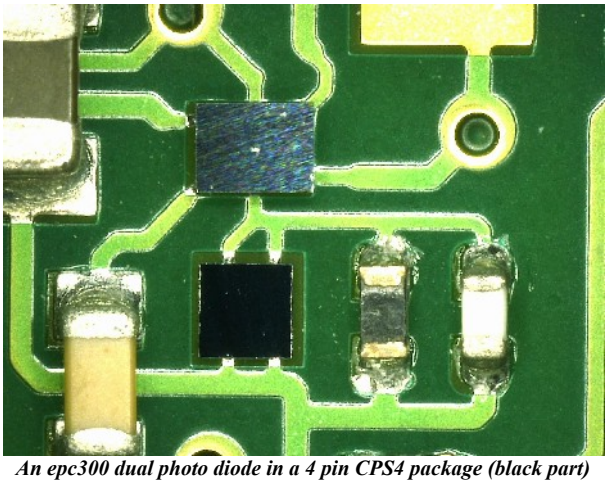
Photo Diode Arrays epc3xx with 2ns Response Time

epc has developed a full line of PIN photo diodes. It starts from a simple 1x1 mm device in a CSP4 package and extends to a device with a size of 2x4 mm containing 16 individually assignable photo diodes (see diagram).



Using chips from the epc3xx product line, linear or two dimensional arrays can be formed for any application, be it triangulation, spot location, angle measurement, rotary encoders, or similar. Also, spectral sensitive detectors can easily be designed by applying color filters in front of the photo diodes.

Also, other sizes are available upon request. It would be possible to manufacture photo diodes of up to 15x15 mm or even bigger. Such a 15x15 mm device then would contain 450 photo diodes, each of them individually accessible. All diodes have in feature a high quantum efficiency of 90%, a reverse breakdown voltage of up to 40 Volts and a response time down to less than 2ns. All devices are available with or without daylight filter for 940nm LEDs.



An epc300 dual photo diode in a 4 pin CPS4 package (black part) on a PCB. The size of the photo diode is 1x1 mm only.

Pricing information and data sheets are available upon request at sales@espros.ch. Samples are available from stock.

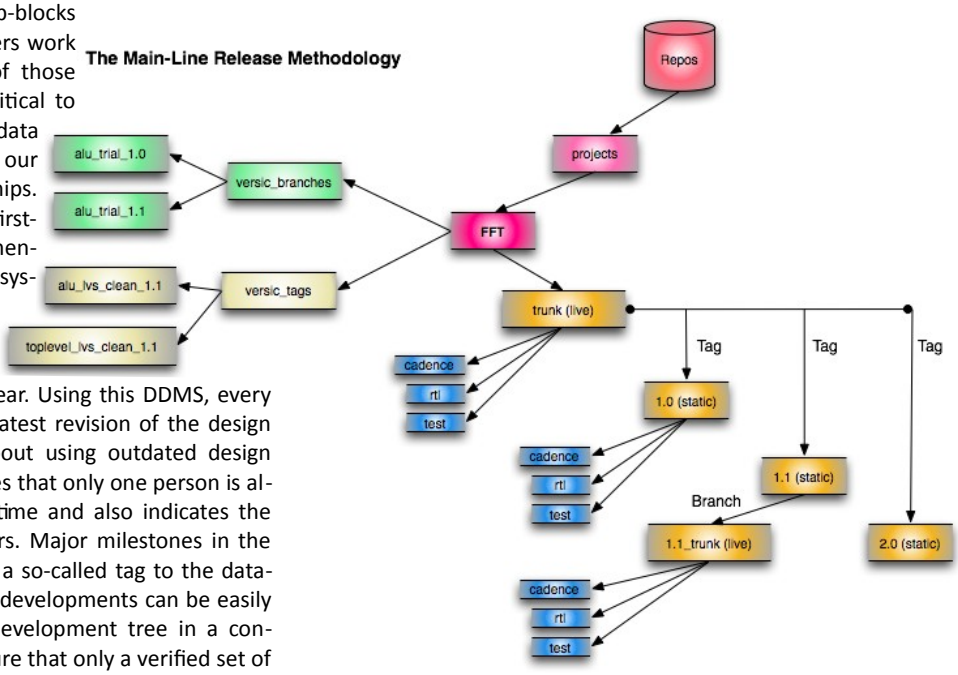
Chip Scale Packages are very small...

Space is crucial in our applications so we constantly seek to increase the integration density. But standard packages partly counteract minimum space through their size. We therefore offer each product in a chip-size package (CSP) which, in fact, is a bare silicon die with its interconnects in a standardized grid of 0.45 or 0.5 mm. The interconnects, we call them “Stud Bumps”, are located on the rear side of the chip. Since these interconnects and the grid are so small and some of the interconnects are hidden, the chips can only be attached to a PCB by reflow soldering. Manual soldering is no longer possible.

In order to make the characterization of prototypes possible, we are currently investigating socketing solutions for CSPs for prototyping purposes. Tailored, product-specific sockets guarantee safe contact with our extremely thin 50µm dies without damaging them. The image to the left shows a dummy bare die in a CSP socket with turn-up lid. The size of the chip is 2x4 mm.

Design-Data Management for Highest-Quality Chips

The latest generations of epc chips already consist of several hundred thousands of electronic devices such as transistors, resistors, capacitors, diodes and other components. They are grouped into many blocks and sub-blocks and up to 10 chip-design engineers work on the schematics and layout of those blocks in parallel. Hence, it is critical to ensure that only the right layout data makes it into the fabrication of our highly integrated opto-sensor chips. In order to achieve our goal of “first-time-right” chips, we have implemented a design-data management system (DDMS) early-on in the creation of our state-of-the-art chip-design methodology, which will be ISO 9001 certified later this year. Using this DDMS, every designer always works with the latest revision of the design and does not have to worry about using outdated design data. A locking mechanism ensures that only one person is allowed to work on a block at a time and also indicates the name of the editor to other users. Major milestones in the design flow are frozen by adding a so-called tag to the database while redesigns and further developments can be easily branched-off from the current development tree in a controlled manner. Besides making sure that only a verified set of mask data goes into production, it also enables us to go back to any earlier version of a design if required for verification and reassurance.



The number of Available Building Blocks is Increasing

Since its foundation in 2007, epc has already developed 6 product lines with a total of not less than 40 different products. These range from simple I/O-drivers for 24 Volt systems to complex photonics chips. Many building blocks had to be designed especially for these products. These building blocks are now part of our toolbox when we develop new standard and customer specific chips. The re-use of already developed blocks speeds up the design time and reduces the risk of design error. Thus, customer specific chips can be developed in a very short time with a high probability of achieving first time right. The following building blocks are already available and are fully characterized.

- Photo diodes and CCD structures
- 3D-TOF pixels and pixel structures
- Low voltage and high voltage transistors
- Poly resistors and capacitors
- EEPROM
- Amplifiers and comparators
- Analog and digital input stages and output drivers
- Voltage and current references and regulators
- Analog and digital filters
- A/D-converters
- Communication interfaces
- Oscillators with or without crystals
- PLL

Customer specific photonics chips come from epc. High performance, short turn-around time and low cost are the key!

+++ test engineer, IP manager, sales engineer, etc. +++ interesting job opportunities on www.espros.ch +++ have a look! +++